

Low Power LCD Driving Scheme

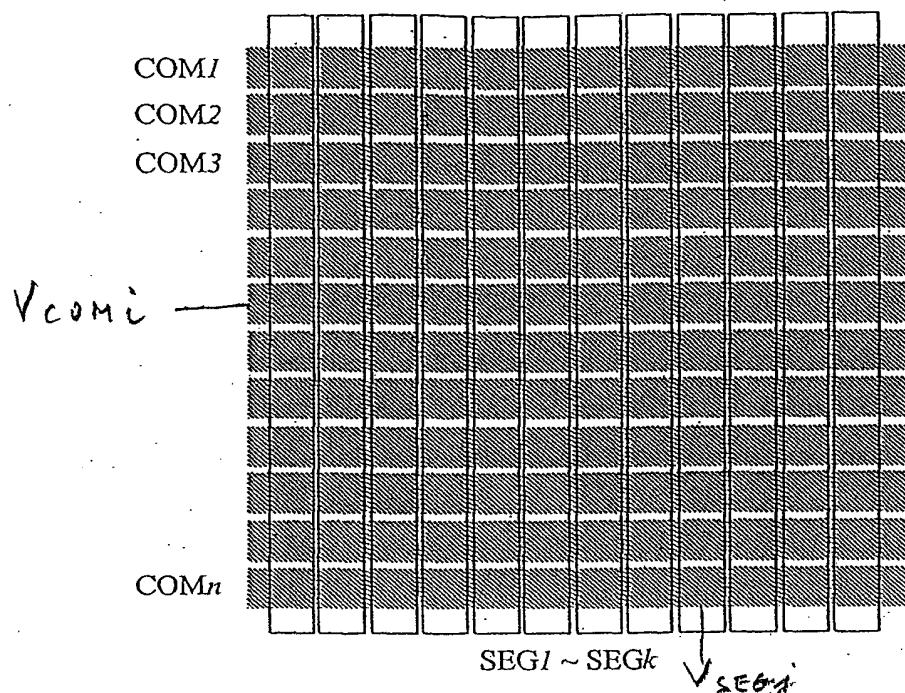


Fig. 1 A see through view of a LCD panel and its ITO electrodes

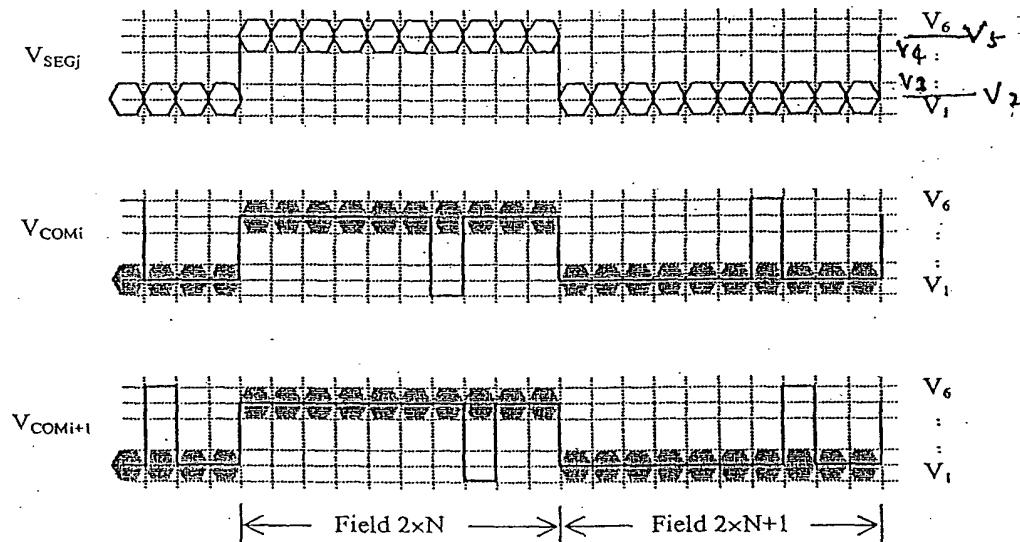


Fig. 2a IAPT driving Wave forms for COM electrodes and SEG electrodes

P R I O R A R T

Low Power LCD Driving Scheme

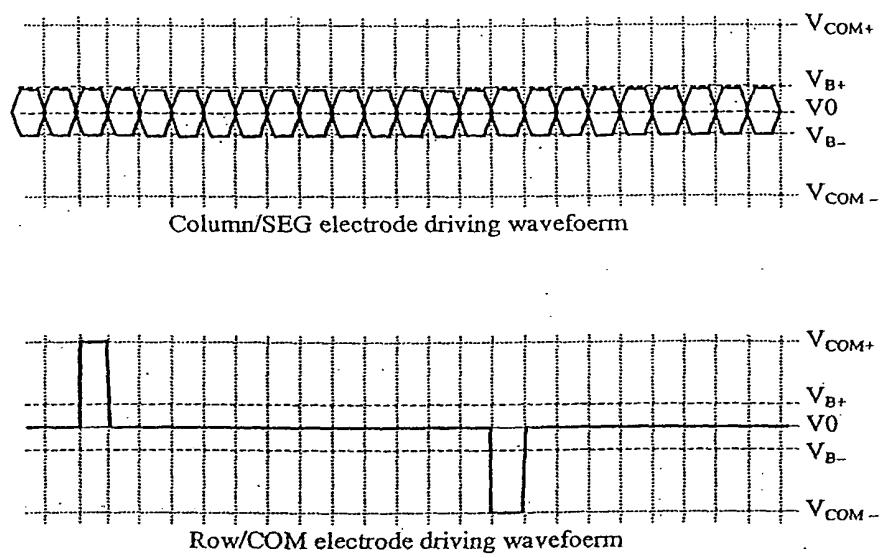


Fig. 2b APT driving Wave forms for COM electrodes and SEG electrodes

PRIOR ART

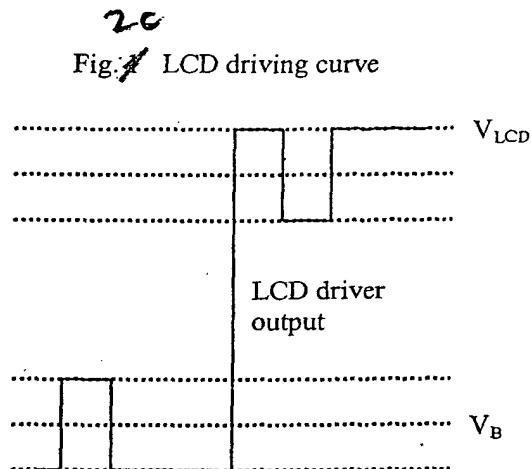
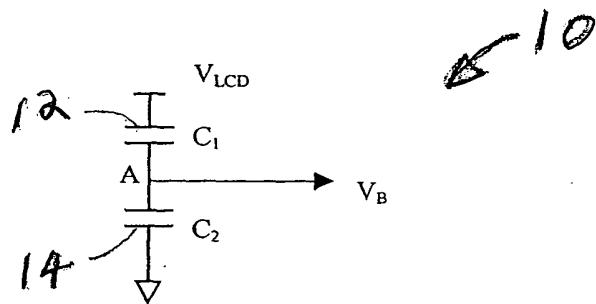
Figures:

Fig. 3 A capacitor bias ratio generation circuit



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Fig. 4. A capacitor bias ratio circuit with periodic refreshing.

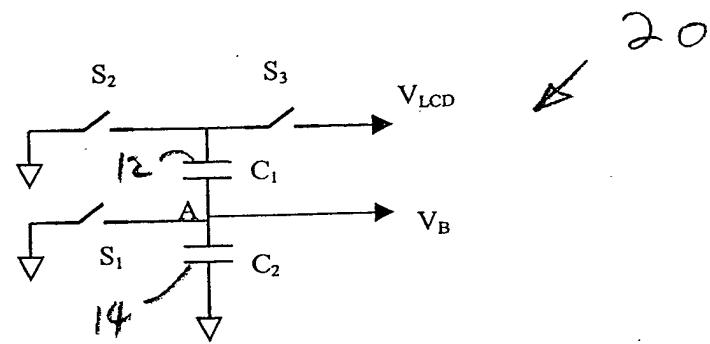
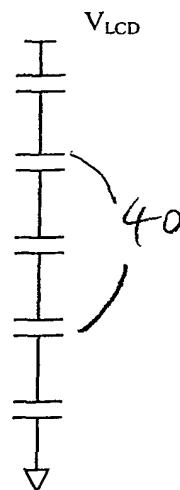


Fig. 5a An alternative capacitor divider bias ratio generation circuits.



Phase 1

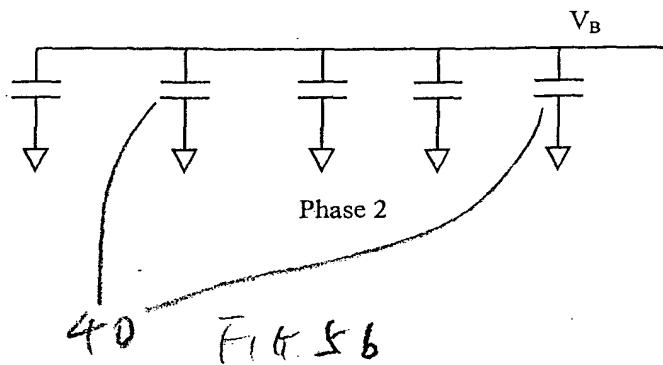
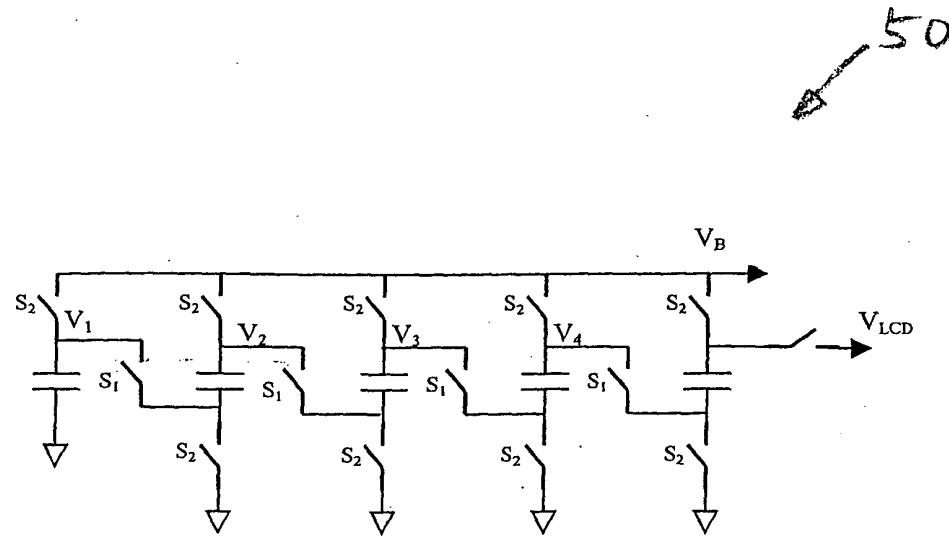


FIG. 5b

Figure 6. Detailed Implementation for Figure 5.



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Fig. 7. Direct Drive Capacitor Divider

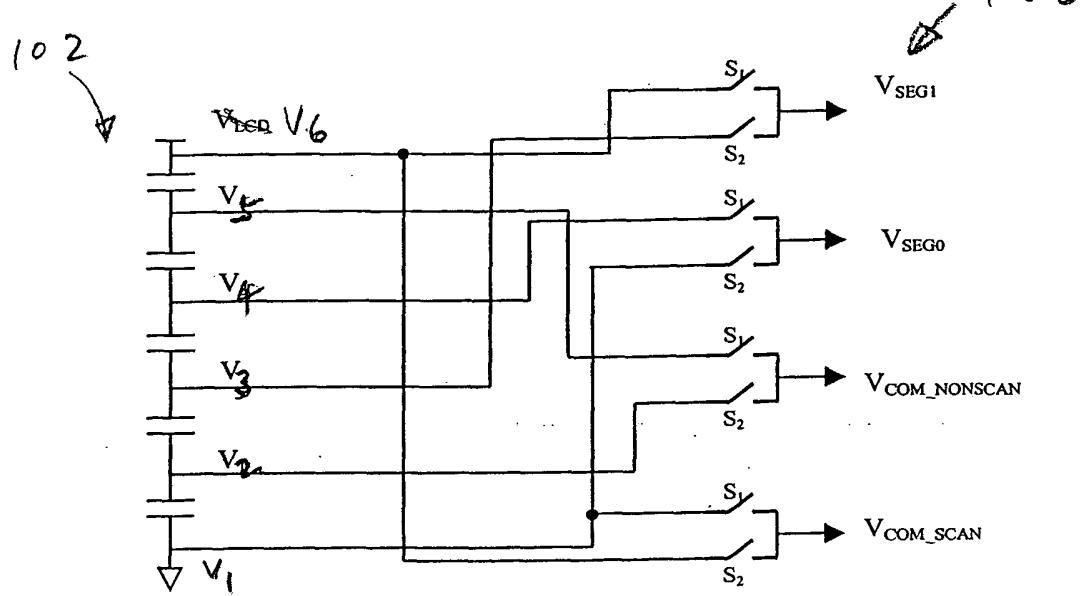


Fig. 8. Direct Drive Capacitor Divider with Four Caps. (BR=4) All the caps are equal.

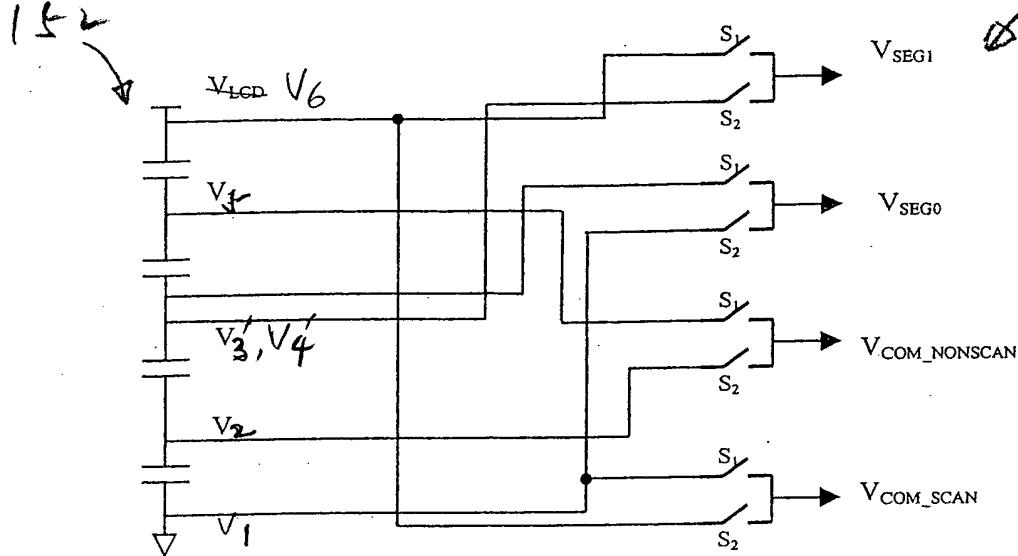


Fig. 9. Direct Drive Capacitor Divider with Three Caps. (BR=3) All the caps are equal.

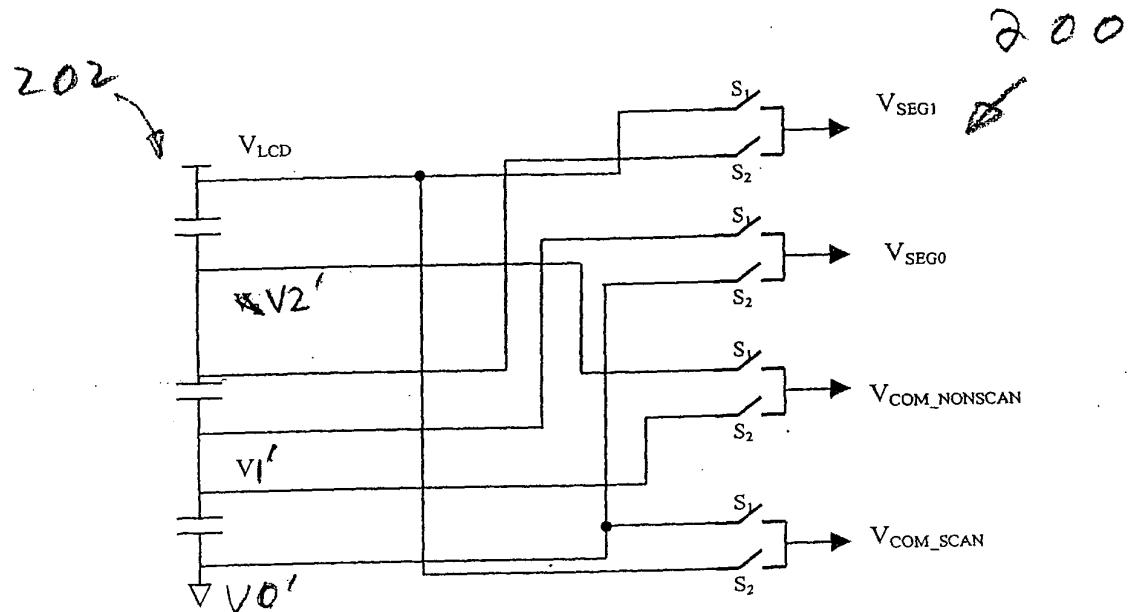


Fig. 10 1/3 LCD driving waveform

	C1	C2
R1		
R2	█	
R3		

